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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,852	01/30/2004	Roderick A. Barman	P388 0008/GNM	3901

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,852	BARMAN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,7,9,15,16,19,20,22-26 and 29-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,7,15,16,19,20,22-26 and 29-32* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 11, 2007 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6-7, 15-16, 19-20, 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamanaka et al., US Patent 4807259, hereinafter Yamanaka.

4. In re claim 1, Yamanaka discloses a method of synchronizing one or more devices on a first bus [associated with master; e.g., 10, 17], the first bus associated with a first clock [17] for generating first bus timing information [e.g., TM] for the first bus [first clock timing information is associated with the elements of master station; i.e., timing information sent over first bus is obtained from first clock] with one or more devices on a second bus [associated with slaves; e.g., 20, 27], the second bus associated with a second clock [27] for generating second bus timing information [e.g., TS] for the second bus [second clock timing information is associated with the elements of slave station; i.e., timing information sent over second bus is obtained from second

clock], each of the devices having an individually adjustable timing [fig.3], the method comprising:

- Acquiring the first bus timing information [e.g., TM] and the second bus timing information [e.g., TS] from the first bus and the second bus respectively [col.7, ll.6-32; timing of components including devices and bus of each station refer to each respective clock].
- Determining a timing offset [TD] between the first bus and the second bus [col.7, ll.24-40].
- Broadcasting the timing offset to the one or more devices on the second bus [col.7, ll.34-49].
- Adjusting the timing of the one or more devices [e.g., 20] on the second bus to be synchronized with the one or more devices [e.g., 10] on the first bus based upon the broadcast timing offset [TD] and the second bus timing information [e.g., time of 27] [col.7, ll.43-49].

5. As to claims 6, 20, 23, Yamanaka discloses, wherein the one or more devices on the first and second buses are each configured to begin an operational cycle according to a rule based on timing information of the first bus [col.1, ll.24-55; measurement at predetermined time in synch with master].

6. As to claims 7, 24, Yamanaka discloses, wherein the one or more devices on the second bus adjust their timing by determining timing information of the first bus by applying the timing offset to the timing information of the second bus [col.7, ll.42-47].

7. As to claim 15, Yamanaka discloses, comprising automatically broadcasting timing information on the first and second buses [col.7, l.62 – col.8, l.2; automatically after adequate timing].

8. As to claim 16, Yamanaka discloses, wherein the method is carried out on a data processor [1] comprising first and second interfaces [part of 18] coupled to the first and second buses, respectively, and wherein acquiring timing information from the first bus and the second bus comprises querying the first and second interfaces for the timing information [col.7, ll.6-25; 18 inherently uses some interface in the broadest interpretation to access master and slave times].

9. In re claim 19, Yamanaka discloses each and every limitation as discussed above in reference to claim 1 [i.e., separate master bus corresponds to the first bus of claim 1 and first and second buses corresponds to the second bus of claim 1].

10. In re claim 22, Yamanaka discloses each and every limitation as discussed above in reference to claims 1 and 16. Yamanaka discloses the apparatus [fig.3] comprising:

- A processing element [10] coupled to the first and second buses by the first and second interfaces respectively [e.g., 29, 39] to receive timing information for the first and second buses.
- A program memory coupled to the processing element, the program memory containing software instructions programmed to cause processing element to calculate a timing offset between the first bus and the second bus and broadcast the timing offset to the one or more devices on the second bus by means of the second interface [inherently, some memory is required to store the instructions in order for 10 to perform accordingly].

- A timing control system [part of 20, 30] in each of the one or more devices on the second bus, the timing control systems each configured to adjust a timing of a corresponding one of the devices [20, 30] based upon the second bus timing information and the timing offset [col.7, ll.43-47].

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 1 above, and further in view of Baker, US Patent 6650719.

13. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose calculating a drift rate of the timing offset.

14. In re claim 3, Baker discloses a method comprising calculating a drift rate of the timing offset and broadcasting the drift rate [col.1, ll.12-49].

15. In re claim 4, Baker discloses, wherein calculating the drift rate comprises calculating a first order time derivative of the timing offset [col.8, ll.8-10; timing offset fed to differentiator with first order filter].

16. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Baker before him at the time the invention was made, to modify the method taught by Yamanaka to include the drift rate calculation taught by Baker, in order to obtain the method comprising calculating a drift rate of the timing offset and broadcasting the drift rate to

the one or more devices on the second bus and adjusting the timing of the one or more devices on the second bus to be synchronized with the one or more devices on the first bus based on the timing offset and the drift rate and the second bus timing information, as drift rates are well know in the art and suitable for use in the system of Yamanaka [digital transmission system]. One of ordinary skill in the art would have been motivated to make such a combination as it provides an important parameter in processing signals in a digital transmission system [Baker: col.1, ll.12-32].

17. Claims 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 22 above.

18. Yamanaka discloses the apparatus wherein the first and second interfaces and the processing element are all located within a data processor [1] configured to process data received from the one or more devices on the first bus and the one or more devices on the second bus [fig.3a].

19. In re claim 25, Yamanaka did not disclose explicitly a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses. Examiner had taken Official Notice that it is well known in the art to set the bandwidth of devices, particularly to set the bandwidth to the maximum allowable bandwidth of the bus used for communication, and that one with ordinary skill can setup the bandwidths so that a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka before him at the time the invention was made, to setup the bandwidths so that a bandwidth of the one or more devices on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses, as the setting of each device's bandwidth to the maximum possible for communication would result in a bandwidth of the one or more devices [e.g., cpu set to use communication bus fully] on the first bus plus a bandwidth of the one or more devices on the second bus exceeds a maximum allowable bandwidth of either of the first or second buses [since cpu is set to maximum of the bus, additional bandwidth of any other device would exceed the maximum of the bus]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to allow each device to communicate at the maximum bandwidth.

21. In re claim 26, Yamanaka did not disclose explicitly the program memory is also located with the data processor. Examiner had taken Official Notice that it is well known in the art to have a program memory be located within some structure [data processor] along with the processing element.

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka before him at the time the invention was made, to have the program memory be located within the data processor, as it is extremely well known [most computer contains a program memory with associated processing element] and suitable for use with the system of Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to group essential elements in an area.

23. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claim 22 above, and further in view of Yagita et al., US Patent 6081324, hereinafter Yagita.

24. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose using cameras in the industrial setting.

25. Yagita discloses the one or more devices that comprise a plurality of cameras, wherein all of the pluralities of cameras are positioned to encircle an image area and to record images of the image area [col.5, ll.31-57].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Yagita before him at the time the invention was made, to modify the method taught by Yamanaka to include the monitoring cameras taught by Yagita, in order to obtain the claimed apparatus. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to monitor foreign materials in an industrial setting such as Yamanaka's [Yagita: col.5, ll.31-57].

27. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka as applied to claims 1, 19 and 22, respectively above, and further in view of Chaudhry et al., US Publication 20020152420, hereinafter Chaudhry.

28. Yamanaka taught each and every limitation as discussed above. Yamanaka did not disclose explicitly a plurality of processors [devices] within each slave station.

29. Chaudhry discloses simultaneously broadcasting the data value [timing offset] to a plurality of devices [redundant processors] on the second bus [170] [0017, 0020].

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Yamanaka and Chaudhry before him at the time the invention was made, to modify the slave stations taught by Yamanaka to include the redundant processors taught by Chaudhry in order to obtain the claimed apparatus comprising simultaneously broadcasting the timing offset to a plurality of devices on the second bus [of the slave stations] and individually regulating a timing of each of the plurality of devices on the second bus based at least in part upon the timing offset. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to tolerate faults in processing systems [Chaudhry: 0016-17; each of the plurality of redundant processors determine the synchronized time - based on the timing offset and the second bus timing information - that can be compared to determine if there is an error].

Allowable Subject Matter

31. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

32. Applicant's arguments filed May 11, 2007 have been fully considered but they are not persuasive.

33. Applicant argues that "TS of Yamanaka's... cannot be both timing information of the second bus and timing of a device on the second bus". Examiner disagrees and submits that timing information for multiple entities may be obtained from a single source.

34. Applicant argues that Yamanaka "fails to disclose 'broadcasting the timing offset...' not necessary in the Yamanaka system because any components in the slave station can use (TS)..."

Examiner disagrees and submits that the timing offset is to be broadcasted initially at least once to adjust the timing [i.e., CPU adjusts the timing according to broadcasted timing offset].

35. Applicant argues that "drift rate described by Baker is a drift rate of a frequency". Examiner submits that Baker, read in entirety, discloses the drift rate [DR] of a timing offset [FO] [col.8, ll.27-28].

36. Applicant argues that Baker "do not appear to be applicable in the context of Yamanaka". Examiner disagrees and submits that both references are involved with the problem of determining accurate timing. Additionally, concepts such as drift rates, offsets, and associated derivative values are well known in communication processing.

37. Applicant argues that Chaudhry "do not have individually-variable timing". Examiner submits that the rejection was based on a combination of Yamanaka and Chaudhry that discloses each and every limitation [Chaudhry: 0016-17; each of the plurality of redundant processors determine the synchronized time as taught by Yamanaka - based on the timing offset and the second bus timing information - that can be compared to determine if there is an error].

38. Applicant conjectures that "if a person attempted to combine Yamanaka and Yagita then the person would either attempt to treat each camera as a slave station and synchronize each slave station..." Examiner submits that the person would just as likely provide a processor for each of the cameras in order to record images with a local time derived from the broadcasted timing offset and the timing information of the second bus [e.g., slave clock].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
July 7, 2007